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BD 980

TECHNICAL

MANUAL

JULY 1986

EVENTIDE INC.
1 ALSAN WAY
LITTLE FERRY, NJ 07643
(201) 641-1200

T A B L E O F C O N T E N T S

SYSTEM OVERVIEW

The Eventide BD-980 Broadcast Delay Line is an advanced stereo obscenity deletion and delay catch-up processor that uses the latest digital signal processing techniques and algorithms to perform its function. Because it is essentially a computer system, it is much different than the usual equipment that is found in the typical broadcast studio.

The BD-980 is like all computers in that it has a central processor, memory, and input/output. However, it is more complex than most since it has two complete computer systems. Figure 1 is a system block diagram.

Each of the two computers is a TMS32010 16-bit microprocessor. These chips are capable of executing 5 million instructions per second, which means that each instruction takes only 200 nanoseconds, including multiplications. This is an order of magnitude faster than almost all other single-chip devices currently available. Each TMS320 has a small internal data memory of 144 16-bit words and an external program memory space of 4096 16-bit words. Up to eight input and eight output ports can be used.

The main difference between the two TMS320 computers in the BD-980 is the input/output circuitry for each. One processor, which is called the memory controller or MC, is mainly concerned with manipulating the digitized audio data. Its input/output ports include a 16-bit Analog-to-Digital Converter (ADC) and 16-bit and 8-bit Digital-to-Analog converters (DACs) as well as 1 048 576 16-bit words of Dynamic Random-Access Memory (D-RAM). The second processor, the Lupine Controller or LC, handles signal-analysis and acts as the master system controller. This unit's input/output ports include an 8-bit ADC, the front panel buttons and displays, a small RAM, a data and instruction EPROM array, and several output ports used for system control.

The two computers are interconnected in what is usually called a processor-coprocessor or host-slave system. The LC is the "host" and the MC is the "slave".

The LC acts as the "host" computer. As such, it is responsible for interpreting the user's actions, such as pressing a front panel button or turning the CATCHUP RATE switch. It also operates the front panel displays. It commands the MC to perform certain operations, such as changing the delay or crossfading between two different delay times. It controls the internal relays, and determines the values of the front panel level pots (using an ADC); and sends these values to DACs which are used for input level setting.

Finally, the LC performs the signal analysis that allows the BD-980 to "catch-up" (increase the delay time) unobtrusively. It is this function which actually uses almost all of the LC's capabilities and is the reason why a TMS320 was used for the LC instead of a simpler microprocessor.

Even though the BD-980 is a computer, there is some analog circuitry. However, this circuitry is limited to input and output buffers and filters, and a digitally operated gain control. Only about 10 of the over 200 integrated circuits in the unit are actually used for audio signals.

What does all this hardware and software do? Primarily, the BD-980 unobtrusively increases the delay time after it has been set to zero by

pressing the DUMP button on the front panel. The delay time is increased in discrete "JUMPS" rather than by continuously adding delay. If the delay were continuously increased, an undesireable pitch-change effect would occur.

When a jump occurs, the amplitude of the audio signal at the current delay time is gradually reduced to zero and the signal at the new delay is gradually increased to full amplitude. This crossfade eliminates the "click" that would occur if the delay had been changed abruptly.

However, crossfading between signals with different delays leads to phase cancellations or "glitches" in the output signal. One way to eliminate this is to only "jump" when silence occurs. This is satisfactory, except that the time to restore the full delay can be very long if there are few pauses in the source material. Alternately, the signal can be analyzed for pitch content. If one knows the pitch, the exact length of the jump can be modified so that the crossfade is mixing signals which are in phase. Thus, pauses need not be waited for and the delay catch-up can proceed much more quickly.

It also turns out that the pitch detection process used in the BD-980 is an excellent pause detector. Not only will silence be recognized as a pause, but also (reasonably) random noise, such as room or crowd noise or an intake of breath by an announcer will be interpreted as a pause. Since a jump during random noise is equivalent to a jump during silence (uncorrelated or random noise won't cause glitches), maximum length jumps can be made and catch-up speed is again enhanced.

The front panel rotary switch can select between 32 sets of parameters used when catching up. These parameters are arranged in two groups of 16; one group will only allow catchup during pauses (or random noise) and the other group provides a fixed catchup rate which will speed up even more when pauses are detected. Thus, the user can optimize the system operation by judiciously setting this switch. The parameter setting defines the time between jumps and the pause threshold, and some other special values used by the program.

The software for the BD-980 is contained in two EPROMs. There are actually four separate programs: two of them are used during self-test mode and the other two are used when the unit is operating normally. Of each pair of programs, one is for the MC and one is for the LC. The LC loads its own program from the EPROMs to its program RAM for execution. It downloads the MC programs from the EPROMS to the MC program RAM. There is no separate off-line program storage for the MC within the MC's circuitry.

The EPROMs also have a separate area where parameters and text are stored. These are unloaded by the LC as they are needed. For example, the characters seen on the display come from strings stored in the EPROM. Likewise, when a catchup rate is set using the rotary switch, the parameters used are fetched from the EPROMs. This is done so that the small program RAM of the LC is not cluttered up by data. In other words, all of the LC's program RAM is occupied by executable code rather than a mixture of code and data.

The hardware of the BD-980 system comprises six printed circuit boards:

RDT-320: Dual-processor and memory board.
RA610 : Analog Interface board.
AFP : Front-panel board.
RB-2000: Power supply and mechanical support (motherboard).
ASIO : Optional serial interface for remote control.
ARAM : Optional memory expansion.
In a "standard" unit, the last two boards are not installed.

The RDT-320 board has the two TMS32010 processors and the main memory.

The RA610 board comprises the input buffers, input filters and analog-to-digital converter, the digital-to-analog converter, output filters and buffers. This board also has some timing circuitry and has a "subsampler" used in conjunction with the signal analysis process.

The AFP board has six momentary switches of which five are illuminated, an eight-character ASCII display, the parameter switch, the level control pots, the dual bar-graph display, and the options dipswitch.

Both the RA610 and AFP boards can be regarded as peripherals of the RDT-320 board when considering the system as a whole.

The RB-2000 motherboard serves as a mounting platform for the RDT-320 and RA610 boards. Its components also include the system power-supply.

The ASIO board is an optional piggy-back board which mounts on the RDT-320 circuit board. This board is not discussed in the technical manual.

The ARAM board allows memory expansion of up to 10 additional seconds of audio storage per channel. This board is not discussed in this manual.

C O N N E C T O R S

INTERCONNECTS: RDT320
There are four connections to the RDT320. There is a power connector with +5-Volts and ground. There are also two 40-pin interface cables and one 16-pin memory expansion connector.

POWER CONNECTOR: X 0 0 0 0 X X = +5, 0 = Gnd (6-pin Molex male)

MEXP (memory expansion) 16-pin header.

1	3	5	7	9	11	13	15
A6	A3	A0	A4	A2	A5	A1	A7
2	4	6	8	10	12	14	16
A8	BS4	BS5	BS6	CINH	BS7	RAST	WE

Note that the addresses are multiplexed 256K RAM addresses. Invert and buffer RAST and WE and use BS4-7 as nCAS.

CB (control bus) is used primarily for SLOBUS data transfers.

pin	use	pin	use
1	nBIOL (LC sync signal)	2	S2 (SLOBUS select line)
3	LRST (system reset)	4	S3
5	nRSTB (SLOBUS read stb)	6	S1
7	nWSTB (SLOBUS write stb)	8	S0
9	CBD0 (data lsb)	10	+5 V (not a power connection)
11	CBD1	12	gnd
13	CBD2	14	gnd
15	CBD3	16	gnd
17	CBD4	18	gnd
19	CBD5	20	gnd
21	CBD6	22	gnd
23	CBD7	24	gnd
25	CBD8	26	gnd
27	CBD9	28	fp pot (from fp to RA610 bd)
29	CBD10	30	fp pot (from fp to RA610 bd)
31	CBD11	32	remote exit (from RA610 bd to fp)
33	CBD12	34	remote dump (from RA610 bd to fp)
35	CBD13	36	nMBIO (MC sync input signal)
37	CBD14	38	nSYNC1 (MC sync output signal)
39	CBD15 (data msb)	40	nSYNC2 (MC sync output signal)

MB (memory bus) is used for audio data transfers.

1	nWDAC (write 16-bit DAC)	2	nWL (write to 8-bit DAC)
3	gnd	4	gnd
5	gnd	6	nMTST (not used)
7	MDB15 (msb)	8	gnd
9	MDB14	10	gnd
11	MDB13	12	gnd
13	MDB12	14	gnd
15	MDB11	16	gnd
17	MDB10	18	gnd
19	MDB9	20	gnd
21	MDB8	22	gnd
23	MDB7	24	gnd
25	MDB6	26	nADCEN (16-bit ADC outpout enable)
27	MDB5	28	gnd
29	MDB4	30	gnd
31	MDB3	32	gnd
33	MDB2	34	gnd
35	MDB1	36	gnd
37	MDB0 (lsb)	38	gnd
39	FS (sample-rate clock)	40	WE (write enable)

INTERCONNECTS: RA610

There are five connections to the RA610. There is a 8-pin Molex connector with power and two control signals. There are also two 40-pin interface cables and one 16-pin auxiliary I/O port as well as a 14-pin analog I/O connector.

RO1 or power connector: (8-pin Molex)

1	+5VDC	2	Digital ground
3	-15VDC	4	+15VDC
5,6	Analog ground	7,8	VP2 and VP1

RO2 or MB (memory bus) is used for audio data transfers. RO4 or CB (control bus) is used for connection to the RDT-320 board's SLOBUS. The pinouts of these two connectors are provided above.

RO3 or XP (expansion port) is used for connecting the "dump" and "exit" relays as well as the remote dump and exit/ramp-to-zero signal lines. This connects via a ribbon cable to the DIN jack which mounts on the unit rear panel. Note that this jack is more-or-less compatible with the DIN jack on the BD-955 Broadcast Delay with the exception of pins 4 and 6.

DIN XP
1, 2, 13, 14, 15, 16: no connection or spare.

1	3	remote dump (connect momentarily to pin 5 or 6)
6	4	remote exit or ramp-to-zero ("")
7,8	5,6	ground
7	7	exit relay common pin
3	8	dump relay common pin
NC	9	exit relay N.C. pin
2	10	dump relay N.C. pin
5	11	dump relay N.O. pin
4	12	exit relay N.O. pin

Note that the exit relay N.O. pin is closed only when the unit is in EXIT mode and has timed out (e.g. the "flashing message" is active). If you wish, the jack can be rewired to use the N.C. pin instead.

RO5 or Audio I/O connector: (14-pin DIP socket)

1	ch 1 out +	2	output gnd
3	ch 1 in +	4	input gnd
5	ch 2 in +	6	output gnd
7	ch 2 out +	8	ch 2 out -
9	output gnd	10	ch 2 in -
11	input gnd	12	ch 1 in -
13	output gnd	14	ch 1 out -

INTERCONNECTS: AFP
The Control Bus connector, described above, provides an interface to the system "Slobus." There is also an six-pin Molex connector used for power and two control signals.

POWER CONNECTOR (viewed from rear): (6-pin Molex)

<TOP>
+5
+5
DIGITAL GND
DIGITAL GND
VP2
VP1
<BOTTOM>

INTERCONNECTS: RB-2000 MOTHERBOARD.

The Motherboard has five Molex connectors: one is for AC power, another is a harness for the rear-mounted bridge-rectifier and +5 V regulator. The remaining three are detailed above; the power connector for the front-panel board, and the two power connectors for the RDT-320 and RA610 boards.

Regulator Harness P1:

PIN 1: Regulator IN; Bridge rectifier + terminal.
PIN 2: Bridge AC in (2).
PIN 3: Bridge AC in (1).
PIN 4: Bridge - terminal.
PIN 5: Regulator COMMON pin (digital ground).
PIN 6: Regulator OUT pin (+5 VDC).

Note that pins 4 and 5 are jumpered together at the rear panel.

AC Harness P3: rear panel CORCOM connector to RB2000 P3 and front panel power switch.

CORCOM	P3	
F	8	
D	6	
E	4	
C	2	
B		to power switch.
L		to power switch.
H--N		jumper on Corcom

R D T - 3 2 0 C I R C U I T B O A R D

The RDT320 is a dual processor board that can be used to implement delay lines without using dedicated hardware such as counters, adders, etc. The board is a compact 9" x 13" and comprises 140 ICs with room for a spare. There are 2 M-bytes of on-board RAM, organized as 1M-words by 16-bits (64 ICs).

The dual processors are TMS32010 Digital Signal Processor (DSP) chips. They operate with a clock frequency of 20 MHz from a common oscillator. Each 32010 is provided with program memory and a complement of I/O ports. A detailed description of the 32010 is not possible in this manual. However, we recommend that the TMS32010 USER'S GUIDE (SPRU001A) from Texas Instruments be available as a reference.

MEMORY CONTROLLER: The 32010 (U66) is used as the master control element for the MC. It is used to maintain memory addresses (base and pointers) for the data in the DRAM memory as well as to actually operate on the audio data before they are sent to the DAC.

U66 is clocked at 20 MHz from the master oscillator (U1). U1's output is buffered by (52;3>6). The 5 MHz CLKOUT signal (66;6) is buffered (55;9>8) and applied to the rest of the MC unit as BMC (Buffered M.c. Clock). Data bus buffering is handled by ALS245s Us 64 and 65. nMEN and nDEN are ORed in (55;13,12 > 11). If one of these signals goes LOW (54;10) goes HIGH; causing

Us 64 & 65 to reverse their data direction for reading. U56 is used to latch and buffer address lines A0 thru A7.

The I/O decode circuit is used to select which devices are active on the MC data bus as follows:

INPUT PORTS

PORT #	NAME	USE
0	INSTR	read LS670 register 0 (instruction)
1	DATALO	read LS670 register 1 (parameter)
2	DATAHI	read LS670 register 2 (parameter)
3	SPECIAL	read LS670 register 3 (parameter)
4	SYNC2	sync to channel 2 access period
5		unused
6	RDATA	read data from audio bus
7	SYNC1	sync to channel 1 access period

OUTPUT PORTS

0	WALW	write low-order DRAM address for a write cycle
1	WALR	write low-order DRAM address for a read cycle
2	WAH	write high-order DRAM address
3		unused
4	WL	write to subsampler 8-bit DAC
5	WDAC	write to main 16-bit DAC
6	WBL	write to memory bus latch
7	MACK	Acknowledge handshake signal to LC; write response register U44.

For output ports, U51 (AS138) decodes A0, A1 and A2 and is enabled by (52;12). The circuitry for input is a little different. U49, an ALS157 multiplexer, passes A0 and A1 to the LS670s (Ra, Rb). When A3 is LOW and MDEN is HIGH, the nRIL signal (49;7) goes low, reading the LS670s. U50 decodes the four remaining input ports.

The memory addressing circuit on the RDT320 is given an absolute RAM address and decodes between eight rows of 16 256K DRAMs (only four rows are resident on the RDT-320). The RDT320 memory array is connected as a "common I/O" array, using early write cycles to avoid bus contention.

The memory address is written to octal latches Us 67 and 68 (low-order word) and to hex D-FF U69 (4 lsbs of the high-order word). The actual LSB address applied to the DRAMs is FS. Fs is HIGH when channel two ADC data are available on the audio bus, and is LOW when channel one ADC data are available on the audio bus. Fs is used as A0 on the DRAM address inputs.

Note the implication: ADC samples are written in sequential memory locations; even addresses (0,2,4...) have samples for channel 1 and odd addresses (1,3,5...) have samples for channel two.

LUPINE CONTROOLER: The LC is the master controller for the RDT320 board. It has several basic functions; including controlling the front panel and line/dump/exit relays, downloading programs and parameters to the MC, and performing the jump length and silence detection algorithms.

The 32010 used in the LC is U7. It operates at 10 MHz during boot cycles and 20 MHz during normal operation. Its CLKOUT signal is buffered (20;2>3) and is connected to various points in the LC circuitry as BLC (Buffered Lupine Clock). Data bus buffering is handled by ALS245s Us 8 and 9. When U7 is reading port or program memory data, nDEN (7;32) or nMEN (7;33) will go LOW causing Us 8 and 9 to reverse their data direction for reading. Us 10 and 11 are used to latch and buffer address lines A0 thru A10. The program memory used for the LC comprises two bytewide 2-K NMOS RAMs; Us 12 and 13.

PORT ALLOCATION

INPUT PORTS

PORT #	NAME	USE
0	ENPORTS	enable writing to ports
1	RBUS	read data from Slobus
2	ENMEM	enable writing to program memory 0..7
3	CLINT	end MC>LC return handshake
4..7		not used

OUTPUT PORTS

0	WIN	write instruction to MC (reg file 0)
1	WDL	write param 1 (reg file 1)
2	WDH	write param 2 (reg file 2)
3	WSPEC	write param 3 (reg file 3)
4,5		unused
6	WSYS	write to system control port
7	WBUS	write data to Slobus

The system control port is a 14-bit output port (#6). This port is used to control certain low-level functions of the RDT320 that can only be handled by a dedicated port. The port comprises Us 14 and 15.

bit	use
0..3	Slobus device addresses 0..15 (control lines S0, S1, S2, S3).
4	nSRS line: to MC for reset and program download
5	LAWI: to MC for program download
6,7	not connected
8	CNT: LOW to enable external address count, HIGH to disable.
9	WBE: HIGH to enable Slobus data write from '646s, LOW disables.
10	ILV: not used. Wired to (27;1,4).
11	not used (spare)
12	ENHSK: HIGH to enable LC/MC handshake, LOW disables.
13	nINTM: strobe L-H to interrupt MC. Normally held HIGH.
14	nMTST: not used. Wired to MB connector.
15	nBOOT: set LOW to steer 1/2 speed clock to U7 (32010). setting HIGH provides normal clock and restarts U7.

The "Slobus" is used to interface all external devices to the LC. Special timing is provided to extend the write pulse length and data hold time for outputs on the Slobus, and to permit slow access time devices to be read by the fast input cycles of the 32010. The 4 least-significant bits of the system control port are named the "S-bits." Bits S3 and S2 are decoded to select one of four groups of four ports and bits S1 and S0 select one of four ports per group. The complete allocation and use of each port is as follows:

addr SSSS 3210	input mode	output mode	comments
		RDT320 resident ports	
0000	EPROM	unused	EPROM address from counter
0001	CMOS SRAM	CMOS SRAM	SRAM address from counter
0010	unused	unused	
0011	counter value	counter value	r/w address counter
		RA610 resident ports	
0100	unused	ctl port	AIO board bit control
0101	FIFO	unused	read FIFO
0110	unused	test DAC	test port
0111	unused	level DAC	set input levels
		ASIO resident ports	
1000	UART status	not used	
1001	not used	UART Tx data	
1010	not used	UART Tx data	
1011	UART Rx data	not used	
		AFP resident ports	
1100	switches	not used	read switches
1101	not used	lamps	write lamp latch
1110	set CP to left	DL3416	write to dsp; set char ptr to left
1111	not used	wr addr	write CP addr

When the RDT320 is powered up, the program RAM contains g arbage. Before anything else is done, the program must be downloaded from the EPROM. Since the syten control port is cleared on master reset, the EPROM is automatically placed on the Slobus (S = 0000) and the CNT line is set LOW to activate the counters; which are themselves cleared at that time.

Also, the nBOOT signal will be LOW. This switches 2-1 mux U3 (comprising 4 NAND gates) to select a divided-by-two clock for the 32010 (e.g., 10 MHz). Gates in U19 steer the the nMEN signal not to the program RAM's nOE pin, but to (19;5). Therefore, the 32010 reads instructions from the EPROM. The slower 32010 clock is used so that relatively slow EPROMs will work.

R A 6 1 0 C I R C U I T B O A R D

The RA610 board is the input/output interface of the BD-980. The audio I/O timing chain comprises Us 30, 39, 36, 35 and 33 as well as 1/2 of U37 and three inverters from U28. The input frequency is 1/8 of the crystal frequency of the SONY CX20018 ADC, U41. U30 and (28;11,10) produces BCLK at 1.60 MHz.

BCLK is divided by 4 in HC74 U39 to produce FCLK (400 KHz). FCLK is used by U17 (R5609 switched-capacitor filter) and is also divided again in U36; a HC4017. OSH1 and OSH2 are signals for the DAC sample-and-holds. RCLK strobes the shift register data into the onboard latch within Us 1 and 2. U35 divides Fs by 8. Combining OUTs 1 and 4 in (33;4,5,6) produces a series of pulses at 0.25Fs which are used by the subsampler.

The bus logic selects a device on the Slobus data lines (CB port). The logic comprises U27, 3 inverters in U28, 2 AND gates in U31, and Us 32 and 34. The Slobus device addresses for this board are 0100 thru 0111 or decimal 4 thru 7. This range is decoded as follows:

binary	dec	read	write
0100	4	n.a.	bit data latches (Us23 and 26)
0101	5	FIFO	n.a.
0110	6	n.a.	test dac
0111	7	n.a.	level dac

There is one other condition when this board is enabled. This occurs when the Slobus address is 0001 (static RAM on RDT-320) and the control signal FC is HIGH. This condition occurs when the system is reading from the FIFO and writing directly into the static RAM. This is a type of "hardware assist" for the LC on the RDT-320 board.

The two D-FFs in U38 and one AND gate in U31 are used to provide a CPU sync signal. The MC on the RDT-320 board must sync to the beginning of each I/O cycle (defined as the instants when Fs goes either LOW or HIGH). If the MC wishes to sync to channel 1, it strobes the SYNC 1 line (a LC decoded input line). This clears one FF and presets the other, forcing (31;6) LOW. The MC uses this as its BIO input and enters a waiting loop. When (38;3) goes HIGH, Fs is also going HIGH and (31;4) will go high as the FF is clocked HIGH. This sets the MC's BIO line HIGH and the synchronization is accomplished. The operation is exactly the same when SYNC 2 is used; except that the FFs' roles are exchanged.

The BIO mux (U29) is provided to allow the LC several different BIO sources. The BIO input has a possibility of 8 total inputs, selected by the 3-bit BS field from control latch U26. When the BIO address is 000 - 011, the multiplexer is selected ((29;7) is LOW) and one of the following 4 inputs can be used:

000	Fs
001	FIFO notEMPTY flag bit.
010	FIFO notFULL flag bit.
011	FIFO notWRITE input (a source of 80 us pulses for timing).

The FIFO (21) is a register file that accumulates samples which are output from the AD7574 8-bit DAC. The nFF and nEF pins are active-low indicators of FIFO-full and -empty status. The FIFO can be reset by using one of the output port bits at U26. The sign extension port (U22) sign-extends the 8-bit output of the FIFO into a 16-bit word.

The bit output port (Us 23 and 26) is used for control signals and can be written to via the Slobus. Various aspects or functions of this board can be selected or disabled by the port.

bit 0	resets FIFO when LOW; FIFO runs when HIGH.
bit 1	FC: read FIFO to LC when LOW; to SRAM when HIGH.
bit 2	Test point #2
bit 3	PSC: reset prescaler (U35) when HIGH.
bit 4	BS0 BIO select lines.
bit 5	BS1

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bit 6      BS2
bit 7      Test point #1

bit 8      0: dump relay OFF      1: dump relay ON
bit 9      Subsampler input mux bit "B"
bit 10     "" bit "A"   (A&B choose signal to be sampled by AD7574)
bit 11     0: line relay OFF      1: line relay ON
bit 12     0: exit relay OFF      1: exit relay ON
bit 13     notA/B select for level DAC (U54...AD7528)
bits 14,15  not used.
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RA610 AUDIO CIRCUITRY

The input buffers are buffered unity-gain differential amps used for common-mode noise rejection when balanced input signal lines are connected to the BD-980 . Each circuit comprises three opamps in quad opamp Us 55 and 56. The level match circuit for each channel is a variable-gain inverting opamp used to allow for input gain adjustment for each installation (the remaining opamp in each quad).

Us 53 and 54 comprise the digital equivalent of front-panel level controls. The actual front panel pots produce DC values from 0 to 5 Volts which are digitized and used to set D/A converters in U54 to the appropriate attenuation factor via the Slobus. U53 is used as the current-to-voltage converters for the two DACs in U54.

Us 51 and 52 are modular filters with an upper cutoff frequency of 20 KHz. Each filter can have no more than 3 V RMS input and a 6-db loss in signal level results at the output. The frequency response of these filters is essentially flat within the passband UNLESS they are overdriven. They typically have extremely low distortion and noise.

Since the output level of U51 and 52 is rather small, the signal level must be boosted to match the input requirements of the ADC (10 V p-p). This is done in dual opamp U50. Pre-emphasis is added in this stage since the sampling process rolls off the high frequency response of the signal. Also, a DC offset is applied to the signal so that its range is 0 - 10 Volts.

U49 and its associated components comprise a simple, unbuffered peak detector. The maximum output voltage depends on the input gain-setting resistors and the time-constant is set by the capacitor and bleed resistor values. The output voltages of the detectors pass to the front panel via RO1, the power molex cable (signals VP1 and VP2).

The ADC is a SONY CX20018 (U41). The CX20018 operates at a frequency of 89.6 MHz and produces a divided-by-8 output which is use by the timing chain. The data out are in a serial bit-stream synchronized with both FS and BCLK. Audio data are converted by a dual-ramp process which removes charge from the two sample-hold caps. Each channel's conversion occupies 1/2 of the total sample period or 10 us. While one channel is being converted, the other channel's sample-hold ((45;1,2,3) and (46;1,2,3) for ch 1 OR (44;1,2,3) and (47;1,2,3) for ch 2) is active. The circuit of Us 40, (46;5,6,7), and (47;5,6,7) provides feedback signals used to stabilize the DC bias of each channel of the ADC. The OFFSET TRIM pots for each channel are adjusted for the proper initial DC bias of each channel. The two distortion trimpots for each

channel can be used to minimize THD. The DAMP TRIM pots for each channel adjust each sampler's settling time.

The ADC circuit also has two -5 VDC regulators, one (U43) providing a supply to the digital part of the ADC and the other (U48) providing a supply to the analog section. This division provides lower distortion and noise.

The shift registers parallelize the audio data. These HC595's (Us 1 &2) each comprise a shift register and an output tri-statable data latch. Data bits are emitted from the CX20018 every time BCLK goes HIGH. The next BCLK positive-going edge shifts that bit into the register. When 16 bits have been accumulated, RCLK is generated at (33;3) and the latch holds the parallel data word. When the nADCEN control line on the MB connector goes low, the 595s' notG input goes LOW. This causes the data to appear on the MB data lines for direct writing to the DRAMS on the RDT320.

The main output DAC (U5) is a Burr-Brown PCM-52 16-bit unit. This chip typically settles in about 3 us. Note that it uses all three main power supplies. The data for this DAC are latched from the memory bus by Us 3 and 4. The data MSB is inverted for this chip (as well as the 8-bit DAC) since the MC data out is two's complement data.

The main out S/H's comprise Us 6, 7, and 8. Note that they are similar to the input S/H's associated with the ADC in that they integrate the sampled signal on the hold cap.

This stage (1/2 of U9) performs a signal level reduction required for the output smoothing filters. The DAC output is a maximum of 20 V p-p. The OUTPUT SMOOTHING FILTERS cannot accept a signal greater than 3 VRMS so the signal must be attenuated. Us 10 and 11 are modular filters (identical part to input antialias filters) used to smooth stair-steps from the S/H output.

The output level set stage comprises the other half of U9 and allows for a variable output gain. A trimpot for each channel is used to set output levels, which can vary between slightly less than unity gain (unit output / unit input) and hard clipping. U12 and 8 associated transistors form the output power buffers. This stage is capable of driving fairly heavy loads and is specially arranged to provide an electronically balanced output.

8-bit latch U13 holds the 8 msbs of the memory data bus when it is strobed by the MC. These data represent the audio signal that is to be sub-sampled and then analyzed by the LC. 8-bit DAC U14 and its associated output buffer U15 produces an audio signal at the main system sample-rate. Note that the MSB of the data bus is inverted before being applied to the latch, since the data arrives in two's complement form.

U17 is a R5609 elliptic low-pass switched-capacitor filter (S.C.F.). U17 is powered by $\pm$5 Volts. U17's clock is FCLK. The filter's Fc is about 100 times lower in frequency than FCLK or about 4 KHz.

Another 1/4 of U18 is used as a signal limiter. The resistor values shown actually preclude actual hard limiting at the signal zero-crossings; instead, these crossings are increased in slope.

Analog mux U19 is used either as a sample-hold for the limiter output or as a pure switching arrangement between DC voltages that represent the front panel level pot settings. Control bits from U23 are used to select the mode.

U20 is the subsampler's ADC, an AD7574. This chip performs a conversion in about 30 microseconds. The chip is operated in "ROM" mode, for simplicity. Data are read from the chip when nRD (pin 15) is driven low by nWF. nWF returning HIGH starts the next conversion.

A F P B O A R D

This board is the interface between illogical humans and the logical BD-980. It comprises 6 major sections: bus logic, input port, lamp latch, ASCII displays, level controls, and level displays. For the first four sections, the AFP acts as a peripheral of the RDT-320 board's "LC" processor.

There are two connections to the AFP board: the control bus connector (40-pin ribbon cable) and the 6-pin power Molex cable.

The BUS LOGIC section the decodes four S-bits (S1, S2, S3, S4) from the 40-pin control bus connector) to determine which of the four AFP Slobus devices is active to send or receive data on the bus. The decoder comprises Us 13, 14 and inverters in Us 4 and 5 to decode the following ports:

S3	S2	S1	S0	read fcn	write fcn	comments
1	1	0	0	switches	none	read from input port U2 & U3.
1	1	0	1	none	lamps	write to output port U6.
1	1	1	0	cp = 0	display	read : display pointer to left. write: chars into ascii display.
1	1	1	1	none	set addr	write display pointer.

When the S-bits = 1100 the decoder enables the 16-bit INPUT PORT on the bus. The inputs to this port include the 5-bit BCD switch (parameter switch), the six momentary pushbuttons, and five dipswitches for option settings.

When the S-bits = 1101, data can be written into the LAMP LATCH, U6. The outputs of this latch are buffered by 75452 power drivers and illuminate incandesent lamps within some of the switches.

When the S-bits = 1110, the ASCII display is enabled at both modules' notCE4 pins. Also, U15 (the character position counter or "CP") is enabled for counting. The ASCII display comprises two DL3416 quad ASCII display modules, Us 8 and 9. These are "intelligent" displays, designed for a computer bus. Each character has its own RAM to hold display data.

The A0 and A1 pins are used to select one character within the module as follows:

```
A1     1 1 0 0
A0     1 0 1 0

     ----------
     |        |
     | 3 2 1 0 |
     |_________|
```

The CP is a counter (U15) used to set the A0 and A1 addresses and to manipulate the chip enables to decide which module is active. If the counter is cleared by reading from S-address 1110, the three address bits as output from (4;2,4,6) are HIGH. The bit from (4;2 <the msb>) activates U8 at its chip enable input (8;1), and other two bits select the leftmost character. A write on the Slobus will now write into the left character of the 8-character display. When the write completes, U15 is clocked to count UP and the CP output (after inversion) is now 110 (note that the output counts DOWN). The next character will thus be written to the next-to-leftmost position in the display, and so on.

The LEVEL CONTROLS are two screwdriver-adjust log taper pots connected between +5V and ground. The pot wipers connect via spare conductors on the control bus connector to the RA610 board's analog multiplexer and ADC.

The LEVEL DISPLAY comprises two LM3915 log-taper bar-graph drivers and the two bar-graph displays. The inputs to these chips are the peak-detected input signals (a varying DC voltage) which originate on the RA610 board (VP1 and VP2).

R B - 2 0 0 0 M O T H E R B O A R D

The RB-2000 motherboard circuitry is restricted to a three-voltage power-supply. Both power transformers have their primaries connected to the RFI filtered rear panel AC connector. The connections are made through a harness which plugs in to the bottom of the motherboard. This harness also includes the wiring for the front panel power switch. The rear panel AC connector has a integral fuse holder and voltage switching card for dual-voltage (120 VAC or 230 VAC). The ventilation fan is connected across one set of primaries and has a series capacitor to slightly slow down the fan for reduced noise.

The larger DST 7-16 transformer's secondaries are wired in parallel for increased current. The AC voltage is rectified by the full-wave bridge rectifier on the rear panel. The output of the rectifier is filtered by the two larger caps in the group of four behind the DST 7-16. The filtered DC is regulated to 5 Volts by the LM323 regulator on the rear panel. The rectifier and regulator connections are made through the wiring harness which plugs in at the top right-rear of the motherboard. The +5 Volts is used on the RDT-320, the RA610 and the AFP boards.

The smaller DST 6-36 transformer's secondaries are each connected to a bridge rectifier, filter cap, and + or - 15 Volt regulator to provide the analog supplies for the RA610 board.

The Molex connector on the top right-front of the RB-2000 connects to the AFP board. There are two connections for ground, two for +5 Volts. The signals VP1 and VP2 also are carried on this cable. These signals are used to activate the front panel bargraph display drivers.

BD980 ALIGNMENT

The alignment of the BD980 has essentially four parts: setting up the proper input and output levels, aligning the A/D converter, aligning the subsampler, and adjusting the front-panel displays.

EQUIPMENT NEEDED:
Oscilloscope: Audio bandwidth is acceptable. 10MHz or greater is better.
Distortion analyzer and low-distortion oscillator.
Decade attenuator.

NOTE 1: If pots P3 or P9 for ch 1 or, for ch 2, P4 or P11 are completely misadjusted, the signal to the unit's output will be very distorted due to incorrect operation of the A/D converter.

NOTE 2: Be sure that your scope, oscillator, analyzer, and BD980 are grounded together correctly.

NOTE 3: Items in brackets are channel 2 pin numbers and pots.

Remove the top and bottom covers and position the unit upside down with the front panel facing you. The board you should see is the RA610 Analog and Digital I/O board. It is easily identified by the four vertically mounted filter modules. Look at the diagram of the adjustment pots in fugure 9 and locate the small tri-pots P1 through P14 and ICs 50 and 8.

1) Turn on the BD980 power and initiate the SELF TEST mode. Set the MENU to Fp pots, execute the test and set ch 1 and ch 2 to 72. This is a critical setting. Watch for a minute to ensure they don't drift.

2) Exit the SELF TEST mode and put the BD980 into MANUAL DELAY with delay time at zero.

3) SET INPUT LEVELS: Connect a low-distortion oscillator to both channels 1 and 2 rear-panel XLR input jacks. Note that the input should be connected to pin 3 with pins 1 and 2 grounded. Adjust the input signal to +20 dBm at 1kHz.
OBSERVE: Connect the scope probe to IC 50, pin 1 [IC 50, pin 7]. There should be a sine wave ranging from 0 to +10 volts. If this is not the case, adjust pot P1 [2] (ch 1 [2] input level match) so that the signal is as specified.

4) Connect the scope probe to IC 8 pin 1 [IC8 pin 7]. If no signal is seen at these points P3 and P6 [P4 and P5] may be grossly misadjusted. Turn P6 [P5] if only part of the sampled sine wave is seen and P3 [P4] if the waveform is very distorted on the top. Properly adjust damp trim P3 [P4] by turning it counterclockwise until the signal breaks up. Turn the pot back until the signal is clean then 5 degrees more rotation.

5) Set offset pot P6 [P5] for symmetrical clipping.

6) Readjust input level match pots for 20v peak-to-peak (as close as possible) it IC 8 pin 1 [7]. Readjust offset pots as necessary.

7) Adjust output level pots P13 [P14] for 20 dBm output.

8) Connect scope probe to IC 45 pin 7. Adjust P9 until bottom of signal is between -2 and -3 volts DC. Adjust P11 for same signal at IC 44 pin 7.

9) Adjust 1kHz output distortion with P8 [P7]. Distortion should be below .03%. If clipping (ringing) is observed in the distortion residual turn down the appropriate input level match pot slightly until distortion is as specified.

10) Check distortion at 100Hz. It should be about .05%.

11) Check distortion at 10kHz. It should be about .04%. Attenuating the input level 3db may be necessary to stop clipping.

12) Check 1kHz distortion with input level 30db down (-10 dBm). It should be .3%.

13) Check noise floor, 80kHz and 400Hz filters in on distortion analyzer. This should be -65 dBm or lower. Turning damp trim pot P3 [P4] may lower this slightly.

14) Readjust output level to unity gain (+20 dBm).

15) Check common mode rejection (if desired) on each channel. Input +20 dBm to both + and - phase of XLR. Output level should be -20 dBm or lower.

16) Check frequency response with +14 dBm input. Should be ±1 dBm from 20Hz to 20kHz.

17) Adjust DEGLITCH pot P12 as directed in SELFTEST.

18) Repeat steps 3 thru 16 for channel 2. Items in brackets are ch 2 pin numbers and pots.

19) Turn the unit off and on again and allow the unit to begin normal operation. Be sure that your input level is correct at +20 dBm. Check the output at each XLR and be sure that it is not clipped. A properly adjusted unit should now be just below the threshold of clipping. To verify this, INCREASE the external signal by 1 db. If the unit does NOT clip on both channels, repeat steps 3 and 4 for each channel. You should also repeat step 7 for each channel. Be sure that the unit is in DELAY-ONLY mode before attempting these steps.

20) REDUCE the input signals by 2 db. ADJUST the two pots on the left-top side of the front panel (they are marked for each channel) so that for each bargraph display, all the segments come on. Turn each pot in the opposite direction until the TOP element of each display goes off.

21) If desired, run the extended self-test by holding down the LINE IN button while the unit is signing on. See the operators manual for further information.

USING SELF-TEST TO AID TROUBLESHOOTING

The self test program tests many features of the BD-980. Hidden from the user is the sequence of events occurring during each test. In this section, the meaning of each test is discussed as an aid in troubleshooting.

If the tests work at all, that is, if you can interact with the front panel and select tests, etc., it implies that most of the features of the LC processor are working. The LC is booting up, it can read from the EPROMS, the Slobus circuitry is working, the alphanumeric display works as well as its decoder on the AFP board, and the front panel input port is operating.

BUTTONS, DIPSWTCH and ROTRY SW are all tests that use data obtained from the 16-bit input port on the AFP board. The tests repeatedly fetch data from the port, extract the bit field appropriate for each test, and display the relevant information. Each iteration of the test includes these steps: set the Slobus to the input port address, get a word of data, switch the Slobus to the address counters (RDT-320), set the counters to the address of a message for this test, read the message into the LC's data RAM, switch the Slobus to the front panel alphanumeric displays, set the CP to the left by doing a read from the Slobus, and write 8 characters to the display.

The MEMORY test downloads a special program to the MC. Until the memory test function is activated (when its help message is displayed), the MC program is the normal "audio" program. Once the memory test program has been downloaded, it is active until a QUIT is performed or until the unit is reset.

The MC memory test program has two states: waiting and active. When the test first begins to execute, it is in "wait" mode. Wait mode is a short loop that maintains the RAM refresh until the MC is interrupted by the LC. Hidden from the user is the fact that wait mode is also writing an ascending series of numbers to the 16- and 8- bit DACs on the RA-610 board. The DAC outputs will thus appear as sawtooth waves. This feature is useful to see if the DACs are operating properly.

When the MAX DELAY button is pressed to end the help message, the LC interrupts the MC, beginning the memory test's active phase. Three parameters are passed in the LS670 registers: the beginning row number of the test (4, 3, 2, or 1) and the data to use (2 16-bit words). The MC fetches these parameters, then responds to the interrupt by writing a code to U44 which indicates that it is beginning to write to the memory. Memory is always written to in a descending fashion; from higher to lower addresses.

The LC is itself interrupted when U44 is strobed. It receives the code and displays WRITING etc. on the front panel. When the MC program has written to all the memory from the top of the selected row to the bottom of memory, it writes a "reading" code to U44. The LC is interrupted and displays "READING." If no errors are found, a "passed" code is written to U44, and the LC is interrupted and displays PASSED, etc. If an error occurs, the MC writes a code to U44 which signifies the row and column number of the error. The LC is interrupted, and uses the code to formulate the displayed error message.

After each pass, the MC program returns to wait mode until it is commanded to begin a new test by the LC. This can be seen as a resumption of the DACs' sawtooth waves, which are not active during the actual memory test.

When the user stops the memory test, the current test completes (in the MC section) and then the MC program remains in wait mode until the memory test is again selected; or until the QUIT function is used. However, the output of sawtooth waves to the 8-bit DAC is inhibited. This is done so that the DEGLTCH test can be performed correctly.

During the memory test passes, the numbers written are passed from the LC to the MC via the LS670s. Each pass uses two numbers which are complements of each other. One number is written to odd locations and the complement is written to even locations. This aids in detection of shorts between bit-lines. This memory test is NOT very good at detecting shorts on address lines, which

must be found manually.

The sequence of numbers which are passed to the MC are derived from a 16-count group. The sequence within a group is as follows:

Passes 1 and 2: all ones and all zeroes.
Passes 3 and 4: alternating ones and zeroes.
Passes 5 through 16: random numbers.

The random numbers are formed in a random number generator subroutine that has a periodicity of about 16,384 samples. Note that the CMOS RAM test also uses the same number generator. However, it uses 512 samples during each pass and will cause the random numbers to repeat after 32 passes. This is especially noticable if the ALL TSTS function is used.

If the >MC DEAD message is displayed, it means that the MC is not running and never returns the initial "reading" code to the LC after the MC is commanded to begin the test cycle. This can be caused by several things: problems with the LS670s that interfere with program downloading and parameter passing, problems with the MC's program RAM, or problems with the MC (U66) itself. It is very unlikely that this message will ever appear if the audio program operates correctly. The >MC DEAD failure is called a "fatal error" since the LC will wait for an interrupt that never arrives. The only escape is to press the RESET button or cycle the unit's power.

If a memory error is found and changing the RAM has no effect, there may be some other problem. For example, if the Memory Bus cable (between the RDT-320 and RA-610 boards) is defective, the CPU sync signals (SYNC 1, SYNC2, and nMBIO) may not make it between the two boards (this may also be the cause of an MC DEAD message). In the same way, if the FS signal is missing, the MC cannot discriminate between the two audio channel "time slots" and a memory error will occur. If there are any shorts in the data bit lines on the cable or on either board, a memory error will occur.

If all other tests work except the memory test, and the unit "freezes" if QUIT is used or when the signon completes (and TEST mode is not entered), there is probably a defect in the interrupt circuitry. A "freeze" is seen in one of two ways: either EVENTIDE or QUIT remains in the display, or the NO DELAY message remains in the display and the delay time never begins to increase. For the first case, the LC processor is probably not receiving a BIO signal and is stuck waiting in an initialization code section. For the second case, the interrupt system is defective or the MC processor is "dead."

The DISPLAY test is very simple; it merely writes a number to all 8 positions of the alphanumeric display. However, it works a little differently than the routines which handle message displays. Usually, the CP is cleared to point to the leftmost character and then 8 characters are written. In this test, the CP is cleared at the beginning of the test and then groups of 8 characters are written. After each eighth character is written, the CP should be set to zero as part of its counting sequence. Thus, this test exercises the CP in a way that normally does not occur.

The LAMPS test is another simple test; the lamp latch on the AFP board is alternately set to all ones or all zeroes.

The CMOS RAM test has five parts in each pass. In each part, the CMOS RAMs are tested with a pattern. For the first four parts, the RAMs are tested with all ones, all zeroes, and two alternating patterns of ones and zeroes. The fifth part tests the RAMs with 512 random numbers (same random number generator as used in the MEMORY test).

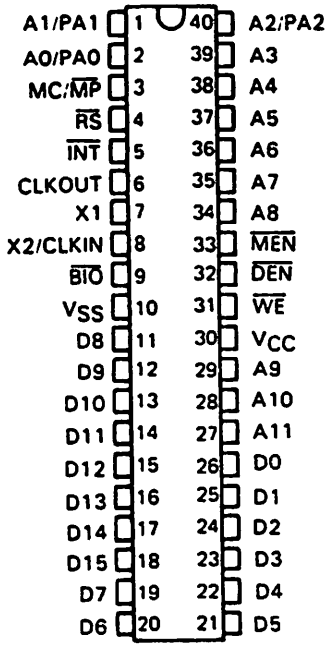
The RELAYS test sets and clears bits in the RA610s U23 to turn the relays on and off. When the LINE relay is tested, it is possible that audio may pass thru the unit and be heard if the memory test has not been used. If it has, a click will probably be heard when the relay is ON, due to the sawtooth wave at the 16-bit DAC output.

The DEGLTCH and FP POTS tests both use the analog multiplexer, the 8-bit ADC and the FIFO on the RA610 as part of the test. The only real operational difference is that the analog multiplexer (U19 on the RA610) is switched to the limiter (U18 pin 14) for the DEGLTCH test and between the two front panel pot connections for the FP POTS test. If these tests work, the analog multiplexer, 8-bit ADC, and FIFO should be OK.

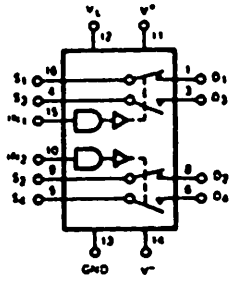
If the unit will not work at all, it is probably not booting up. This may be caused by a bad power supply, by a defective master oscillator (U1), by a short in the EPROM/SRAM address lines or a defect in the address counter itself or its address incrementing circuit, by a defective part in the system control port (Us 14 and 15) or a short on one of that port's outputs, by a defective EPROM, by a short on the Slobus data and/or control lines, by a defect in the Slobus interface circuitry on the RDT-320 or on the AFP or RA610 boards (for example, a device on the AFP is shorting out the Slobus data lines due to a defect in that board's Slobus address decoder). Other culprits may be the LC's I/O port decode and two-speed clock switching circuit, the LC's program RAM, the address and data bus drivers, and the Slobus interface port, Us 16 and 17.

When the "audio" program is running, there are two test points that can be observed for a clue about the unit's operation. These test points are located on the RA610 board, right behind the RO4 connector. Test point 1 has a short pulse every time that the catchup mode program "loop" begins a new iteration. The frequency of the pulse depends on the CATCHUP RATE switch position. This point will stay LOW when the display reads SAFE or if the unit is in WAIT and EXIT or MANUAL DELAY modes. Test point 2 is HIGH during a "crossfade." Crossfades occur during catchup and ramp-to-zero as well as when the delay time is changed in MANUAL DELAY mode. During catchup or ramp-to-zero, a short pulse will also be present if the LC detects silence for the currently analyzed signal.

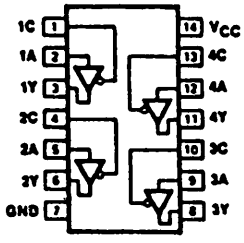
TMS32010JDL - 16/32 BIT MICROPROCESSOR,



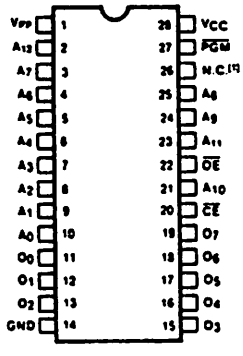
IH5043CPE - DUAL SPDT ANALOG GATE



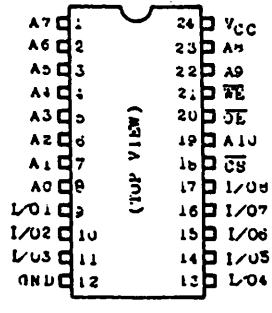
74LS125 - TRI STATE QUAD BUFFERS



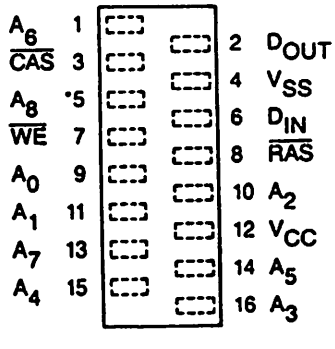
2764 - 8K X 8, 250NS, EPROM



SRM2016C15 - 16K STATIC RAM

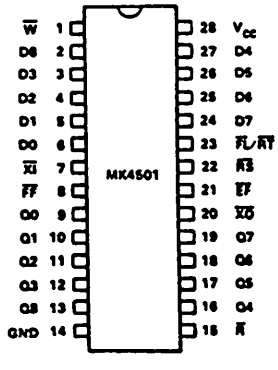


M5M4256L-15 - 256KX1 DRAM, ZIP PACKAGE

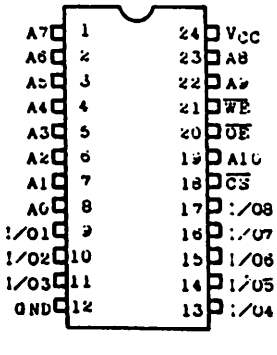


*Address not used for RAS only Refresh

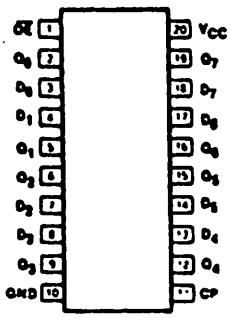
MK4501N-20 FIFO - DUAL ANALOG SWITCH



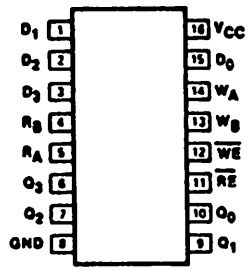
TMM2018D-45 - 8 BIT STATIC RAM



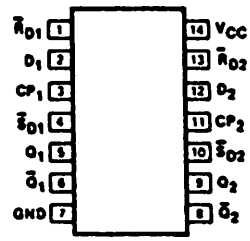
74LS374 -
OCTAL D FLIP FLOP TS



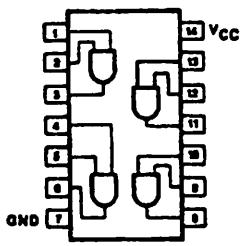
74LS 670 -
4 BY 4 REGISTER FILE TS



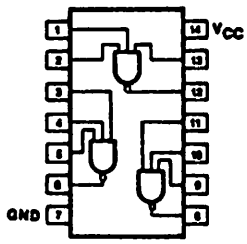
74HC74 -
DUAL D FLIP FLOP
MONOSTABLE MULTIVIBRATOR



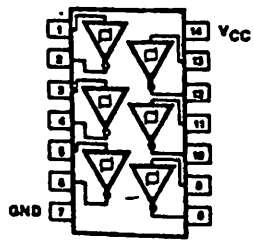
74C08 -
QUAD 2-INPUT AND GATE



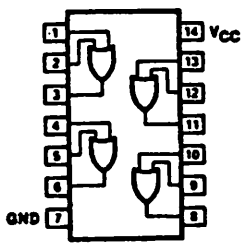
74HC10 - (ALSO 74AS10)
TRIPLE THREE-INPUT NAND
AND GATES



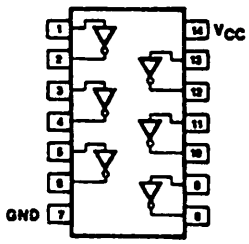
74HC14 -
HEX SCHMITT-TRIGGER
INVERTER



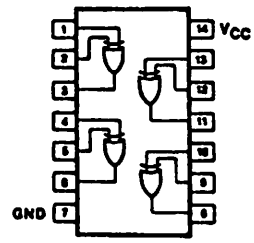
74HC32 -
QUAD 2-INPUT POS-NOR GATE



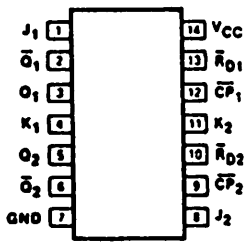
74HC04 -
HEX INVERTER



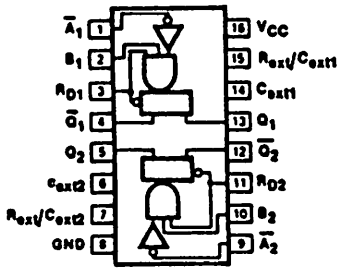
74HC86 -
QUAD 2-INPUT EXCL-OR GATE



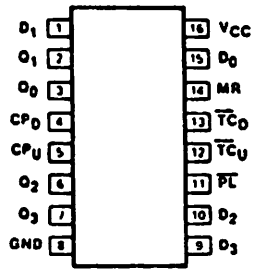
74C107 - DUAL J-K FLIP-FLOP



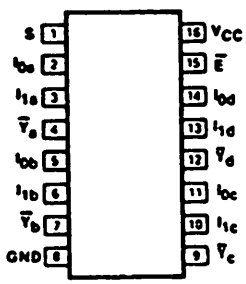
74HC123 - DUAL RETRIGGERABLE



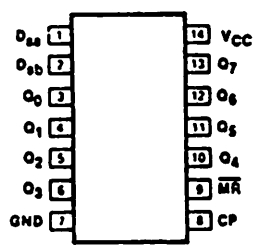
74HC193 - SYNC 4-BIT U/D COUNTER



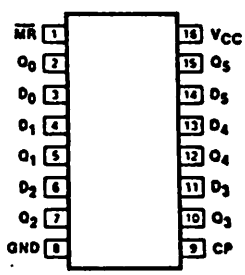
74HC158 - QUAD 2-1 LINE SELECTOR/MUX



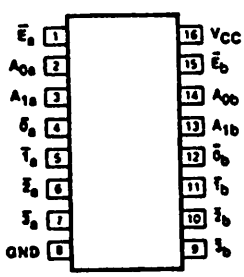
74HC164 - 8 BIT SER IN PAR OUT SR



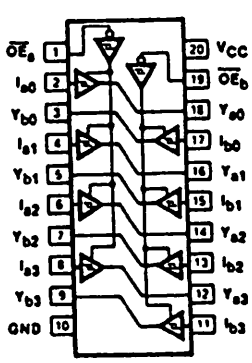
74HC174 - HEX D FLIP-FLOP



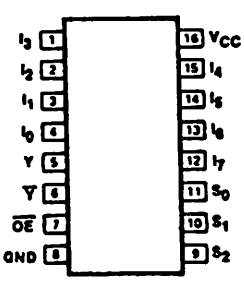
74HC139 - DUAL 2-4 LINE DECODER/MUX



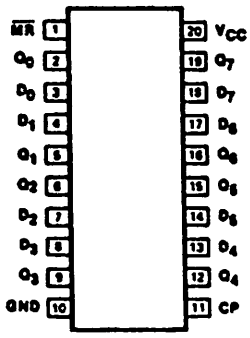
74HC244 - OCTAL LINE DRIVER W/TS



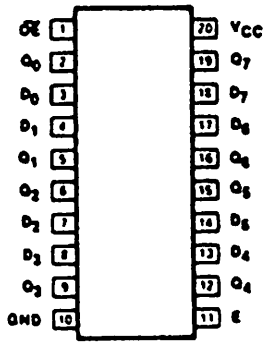
74HC251 - DATA SELECT/MUX 3-STATE



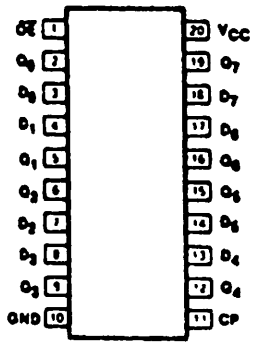
74HC273 - OCTAL D-FLIP-FLOP W/CLEAR



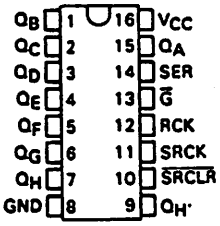
74HC373 - (ALSO 74AS373) TS OCTAL D TYPE LATCH



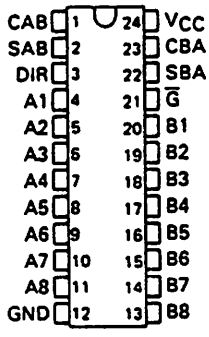
74HC374 - TS OCTAL D TYPE FF



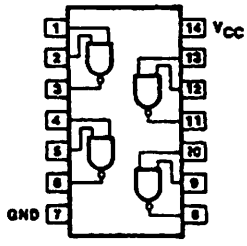
74HC595 - 8-BIT SHIFT REG W/ O/P LATCHES



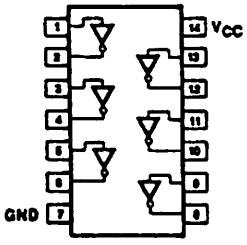
74HC646 - BUS TRANSCEIVERS AND REG



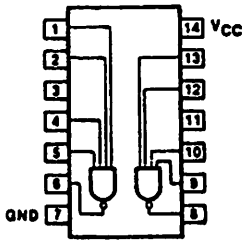
74ALS00 - (ALSO 74AS00) QUAD 2-INPUT NAND GATE



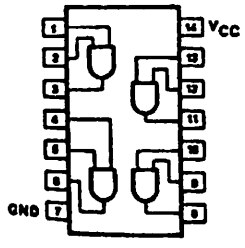
74ALS04 - (ALSO 74AS04) HEX INVERTER



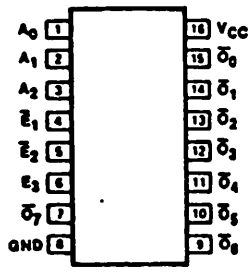
74ALS21 - (ALSO 74AS20) DUAL INPUT GATE



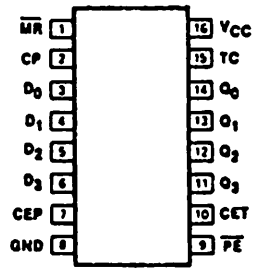
74ALS08 - QUAD 2-INPUT AND GATE



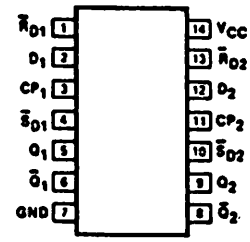
74ALS138 - (ALSO 74AS138) LINE DCDR/DMUX



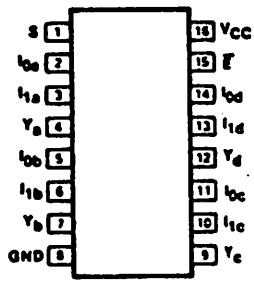
74ALS163 - 4-BIT BINARY COUNTER



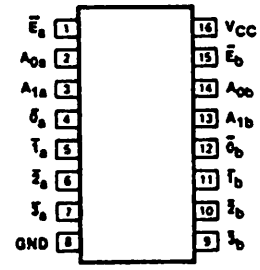
74ALS74 - DUAL D TYP POS TRIG FF



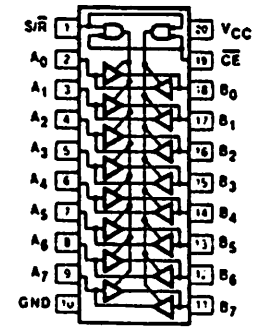
74ALS157 - QUAND 2-INPUT SELECTOR/MUX (INVERTED)



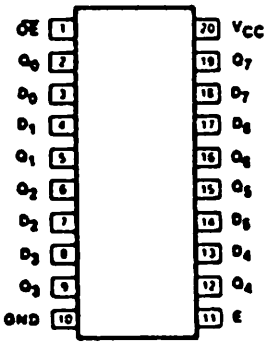
74S139 - DUAL 1 OF 4 DCDR/DMUX



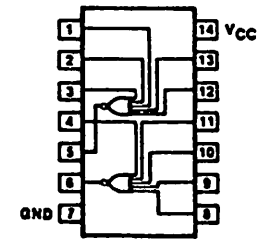
74ALS245 - OCTAL BUS TRANSCEIVER



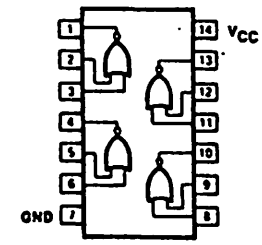
74ALS373 - OCTAL D-TYPE LATCH



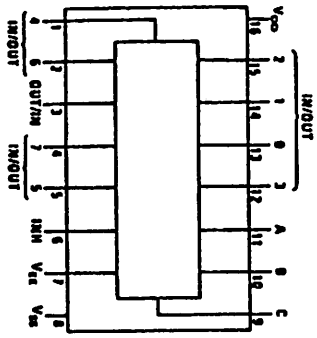
74S260 - DUAL 5 NOR GATE



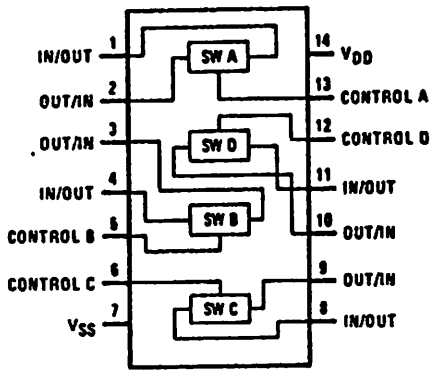
74AS02 - QUAD 20INPUT NAND GATE



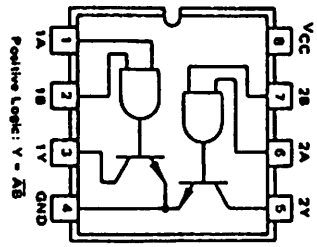
4051 - SINGLE 8 CHANNEL MUX



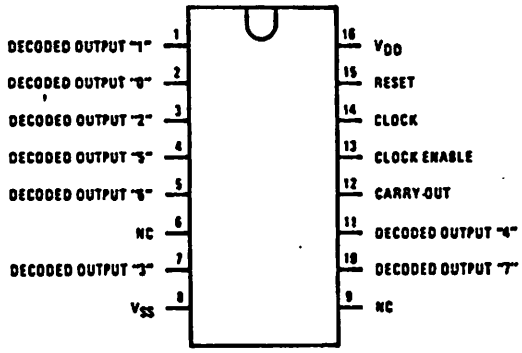
4066 - QUAD BILATERAL SWITCH



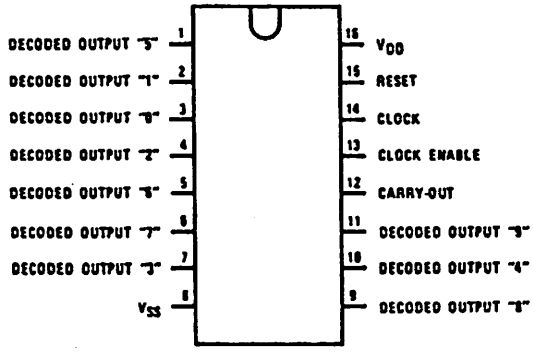
SN75452 - DUAL PERIPHERAL DRIVER



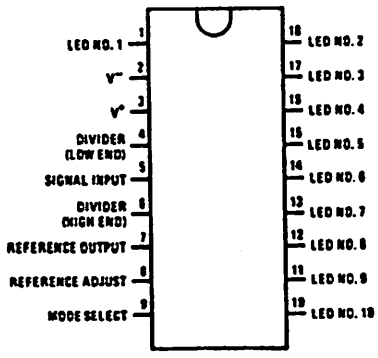
4022 - DIVIDE BY 8 CTR DIVIDER



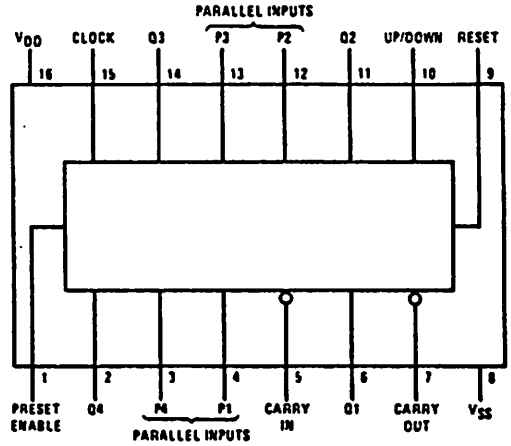
74HC4017 - DECADE COUNTER



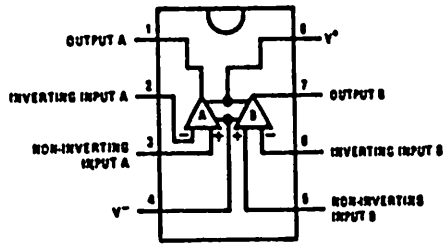
LM3915 - DOT/BAR DISPLAY DRIVER



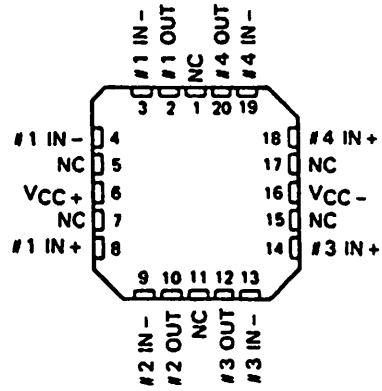
14516 - BINARY UP/DN COUNTER



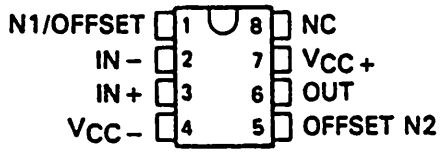
LF 353 -
OP AMP



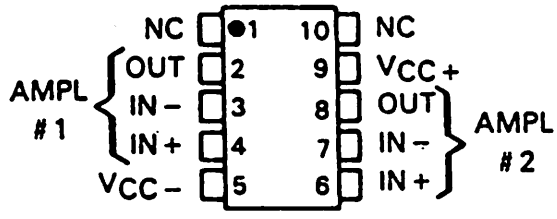
TL064 -
LOW POWER JFET IN OP AMP



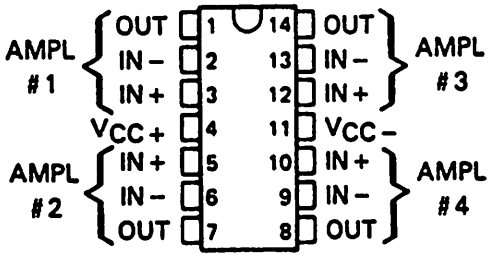
TL071CP -
JFET IN OP AMP



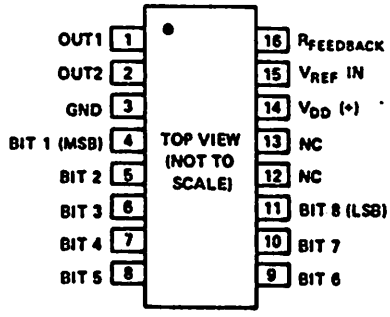
TL062 -
LOW POWER JFET IN OP AMP



TL074 -
LOW NOISE JFET IN OP AMP



AD7523 -
CMOS 8 BIT MUX DAC



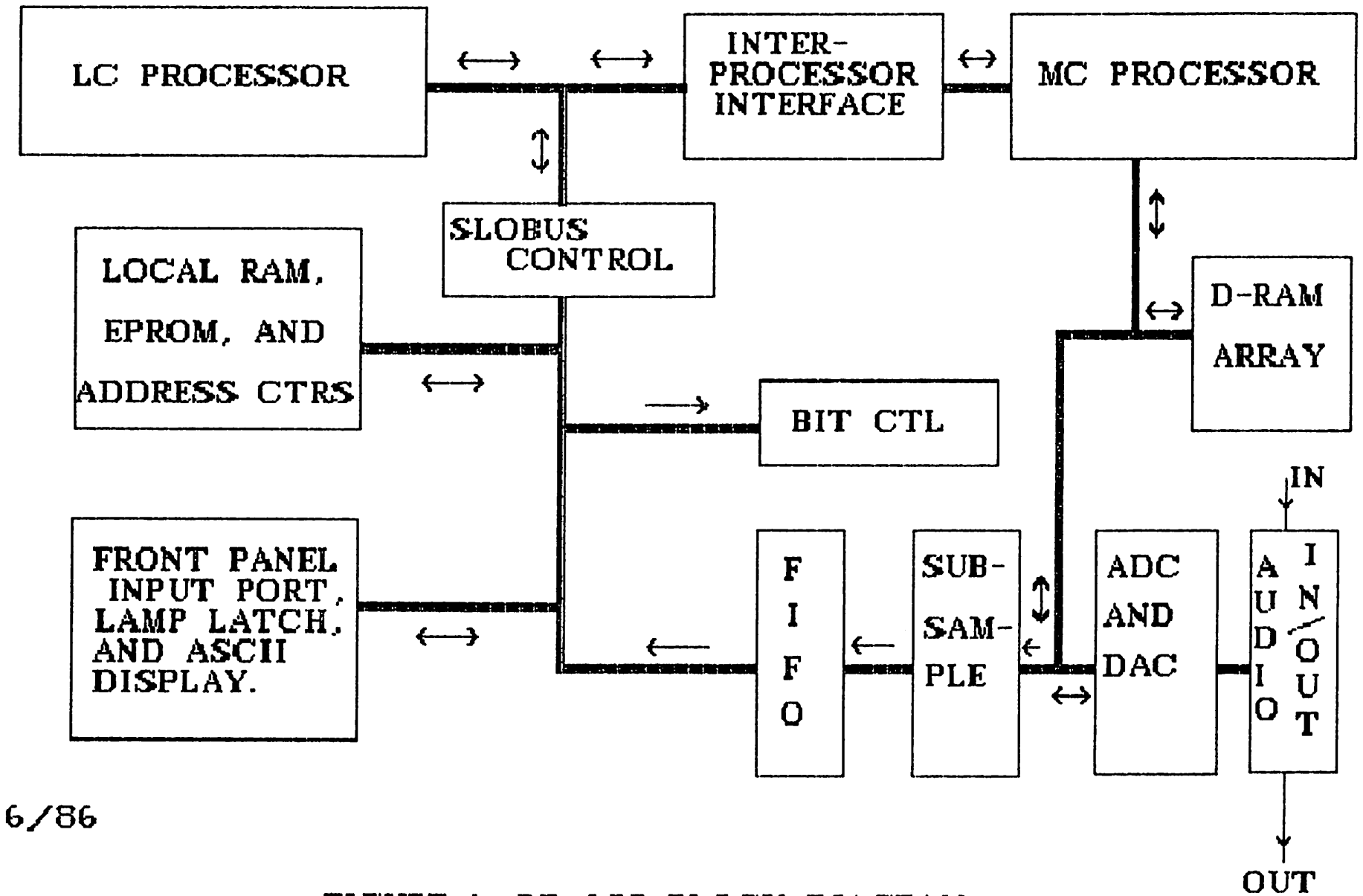


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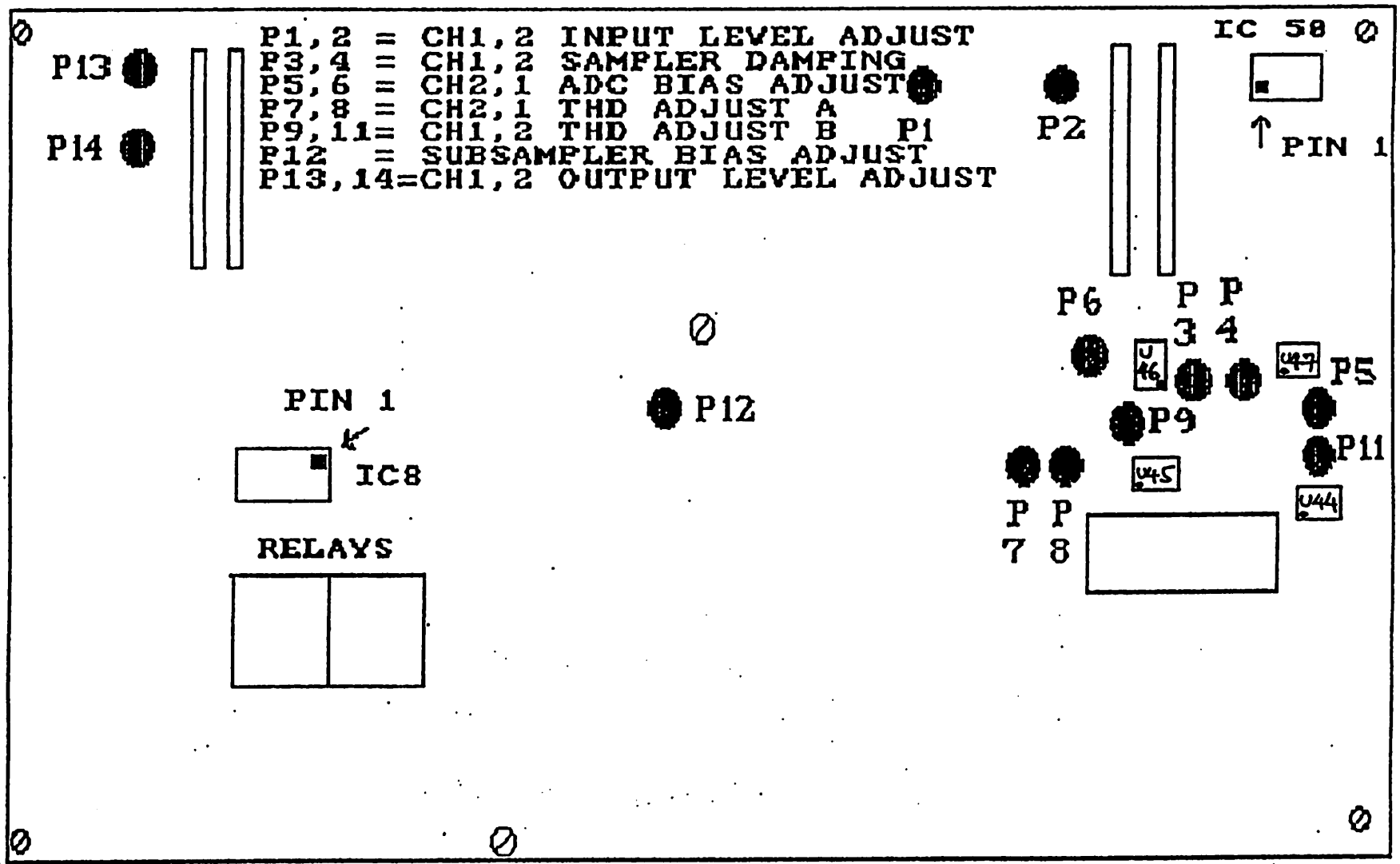
FIGURE 1: BD-980 BLOCK DIAGRAM



NOTE: THERE IS NO P10

FIGURE 9: RA610 BOARD TRIMPOT LOCATIONS 6/86